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Part Number Decoder for Toshiba NAND Flash

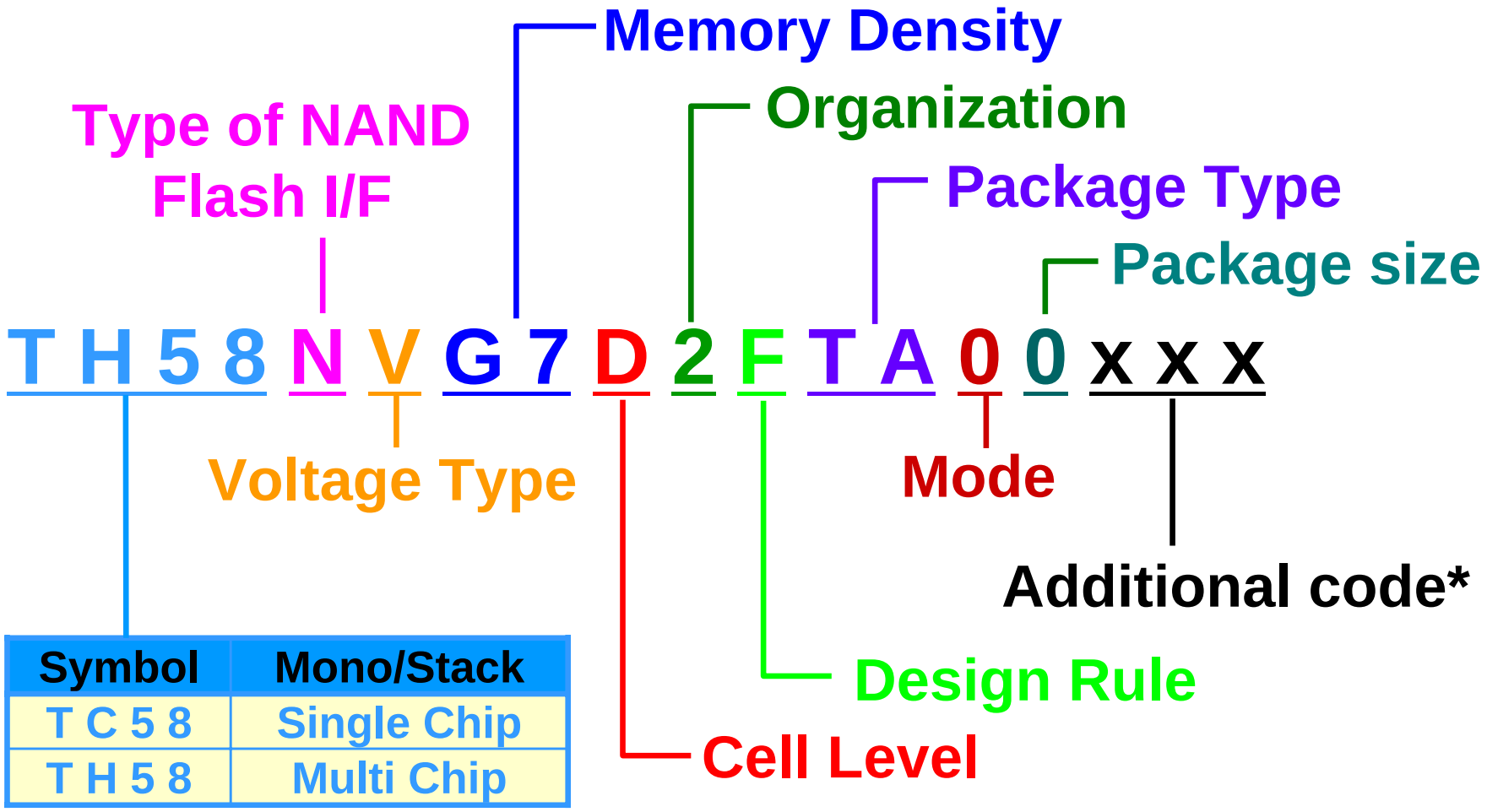
Revision 1.3

Memory Application Engineering Dept.
Memory Division, TOSHIBA CORPORATION Semiconductor Company
Sep.24th'2010

Part Number Decoder
~ Raw NAND ~

This rule is available for 56nm, 43nm, 32nm and 24nm NANDs.

P/N Decoder for Raw NAND(Large Block) ~Definition



Symbol	Mono/Stack
T C 5 8	Single Chip
T H 5 8	Multi Chip

*Part number on datasheet is not including additional code.
Additional code use for Toshiba internal production control.

P/N Decoder for Raw NAND(Large Block) ~Details-1

This rule is available for 56nm, 43nm, 32nm and 24nm NANDs

T H 5 8 N V G 7 D 2 F T A 0 0 x x x

Symbol	Vcc	VccQ
V	3.3V	-
Y	1.8V	-
A	3.3V	1.8V
B	3.3V	1.65V to 3.6V
D	3.3V or 1.8V	3.3V or 1.8V

Symbol	TYPE of NAND I/F
N	NAND
D	NAND *1
T	Toggle mode NAND

*1: Unique character for product variety control.

Symbol	Density
M8	256(=2^8) Mbits =32MB
M9	512(=2^9) Mbits =64MB
G0	1(=2^0) Gbits =128MB
G1	2(=2^1) Gbits =256MB
G2	4(=2^2) Gbits =512MB
G3	8(=2^3) Gbits =1GB
G4	16(=2^4) Gbits =2GB
GA	24 Gbits =3GB
G5	32(=2^5) Gbits =4GB
GB	48 Gbits =6GB
G6	64(=2^6) Gbits =8GB
GC	96 Gbits =12GB
G7	128(=2^7) Gbits =16GB
GD	192 Gbits =24GB
G8	256(=2^8) Gbits =32GB
GE	384 Gbits =48GB
G9	512(=2^9) Gbits =64GB
GF	768 Gbits =96GB
T0	1(=2^0) Tbits =128GB
T1	2(=2^1) Tbits =256GB

P/N Decoder for Raw NAND(Large Block) ~Details-2

This rule is available for 56nm, 43nm, 32nm and 24nm NANDs

T H 5 8 N V G 7 D 2 F T A 0 0 x x x

Symbol	Cell Level
S / H*1	2 Level(1 bits/cell)
D / E*1	4 Level(2 bits/cell)
T / U*1	8 Level(3 bits/cell)

*1: Unique character for product variety control.

Symbol		Page Size	Block Size
x8	x16		
0	5	4KB	256KB
1	6	4KB	512KB
2	7	>4KB	>512KB
3	8	2KB	128KB
4	9	2KB	256KB

Symbol	Design Rule
A	130 nm
B	90 nm
C	70 nm
D	56 nm
E	43 nm
F	32nm
G	24nm A-type
H	24nm B-type

P/N Decoder for Raw NAND(Large Block) ~Details-3

This rule is available for 56nm, 43nm, 32nm and 24nm NANDs

T H 5 8 N V G 7 D 2 F T A 0 0 x x x

PKG	Symbol	Lead Free	Halogen Free
TSOP	FT	No	No
	TG*1	Yes	No
	TA	Yes	Yes
BGA	XB	No	No
	XG*1	Yes	No
	BA	Yes	Yes
LGA	-	No	No
	XL*1	Yes	No
	LA	Yes	Yes

Symbol		Channel	# of /CE	Note
Normal	I-ver.			
0	I	Single	1	TSOP, BGA
2	K	Single	2	TSOP, BGA
4	M	Dual	2	LGA
7	R	Single	4	TSOP PoP
8	S	Single / Dual	4	TSOP, BGA,LGA
A	U	Single / Dual	6	TSOP, BGA,LGA
B	V	Single / Dual	8	TSOP, BGA,LGA

*1: Some of the product are Halogen Free with this code. If necessary, Please ask to Toshiba.

P/N Decoder for Raw NAND(Large Block) ~Details-4

This rule is available for 56nm, 43nm, 32nm and 24nm NANDs

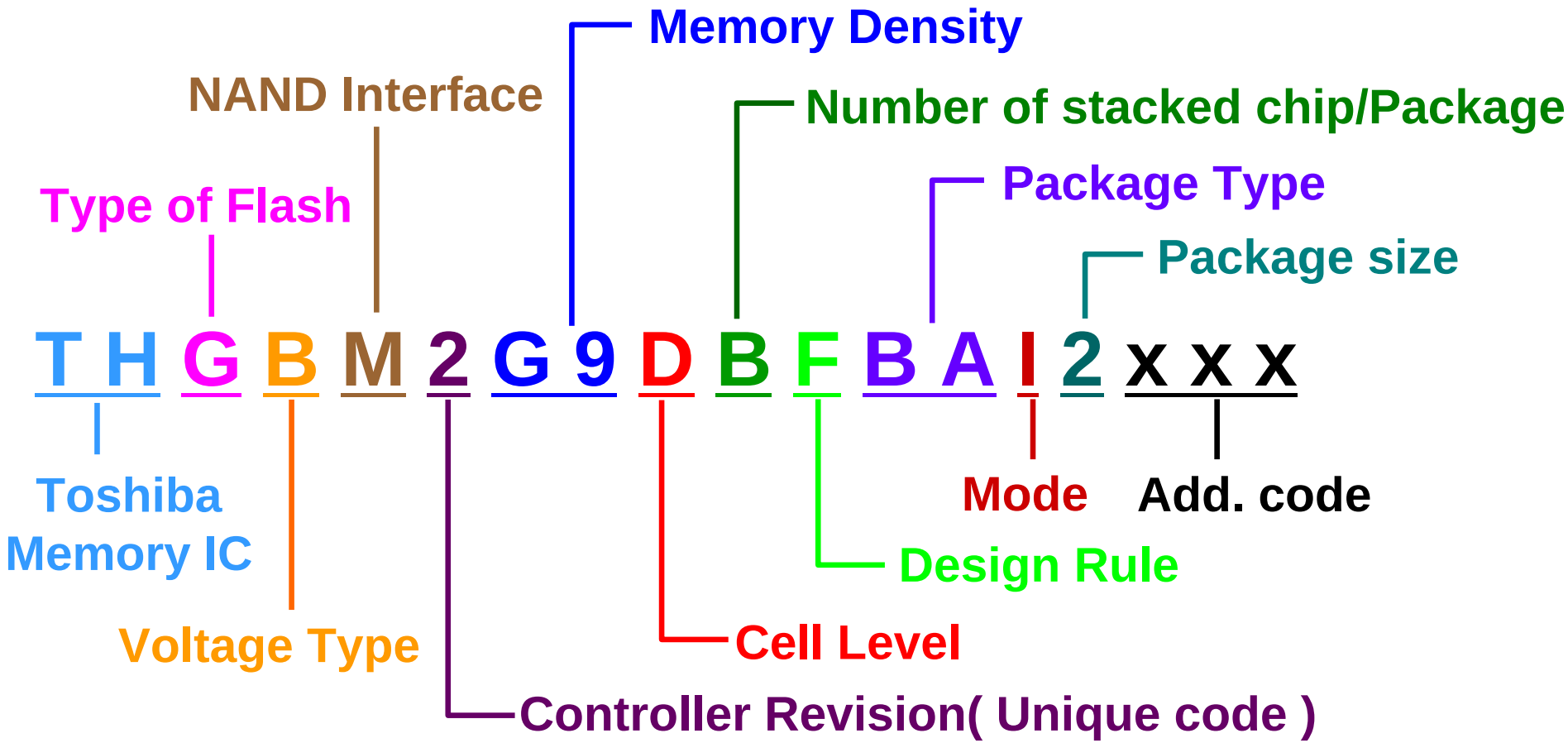
T H 5 8 N V G 7 D 2 F T A 0 0 x x x

Symbol	TSOP [mm]	LGA [mm]	BGA [mm]
0	12 x 20 x 1.2	Reserved	General code(12.5x20, 14x18, 12x18)
1	Reserved	40 lands, 12 x 18 x 0.7	224 balls, 14x18x1.46 *1
2	Reserved	40 lands, 12 x 18 x 1.15	224 balls, 14x18x1.46 *1
3	Reserved	40 lands, 12 x 17 x 0.65	60 balls, 8.5 x 13
4	Reserved	40 lands, 12 x 17 x 1.0	60 balls, 9 x 11
5	Reserved	40 lands, 12 x 17 x 1.04	60 balls, 10 x 13
6	Reserved	40 lands, 13 x 17 x 1.04	60 balls, 8.5 x 13 *1
7	Reserved	52 lands, 14 x 18 x 1.4	60 balls, 9 x 11 *1
8	Reserved	52 lands, 14 x 18 x 1.04	60 balls, 10 x 13 *1
9	Reserved	52 lands, 14 x 18 x 1.0	132 balls(Toggle), 12x18x1.4
A	Reserved	52 lands, 12 x 17 x 1.04/1.0	132 balls(Toggle), 12x18x1.85
B	12 x 18 x 1.2 *1	52 lands, 12 x 17 x 1.4	224 balls, 14x18x1.35
C	Reserved	52 lands, 11x14x0.9	-
D	Reserved	132 lands(Toggle) 12x18x1.04	-

***1: Unique character for product variety control.**

Part Number Decoder
~ NAND with Controller ~

P/N Decoder for NAND w/ controller ~Definition



*Part number on datasheet is not including additional code.
Additional code use for Toshiba internal production control.

P/N Decoder for NAND w/ controller ~Details-1

T H G B M 2 G 9 D B F B A I 2 x x x

Symbol	Type
G	IC
D	Module

Symbol	Vcc	VccQ
V	3.3V	-
Y	1.8V	-
A	3.3V	1.8V
B	3.3V	3.3V or 1.8V
D	3.3V or 1.8V	3.3V or 1.8V

Symbol	Type
M	eMMC
N	NAND
R	PBA-NAND
S	eSD
U	USB
B	Others
C	
D	
H	
W	
X	

Symbol	Density
M8	256(=2^8) Mbits =32MB
M9	512(=2^9) Mbits =64MB
G0	1(=2^0) Gbits =128MB
G1	2(=2^1) Gbits =256MB
G2	4(=2^2) Gbits =512MB
G3	8(=2^3) Gbits =1GB
G4	16(=2^4) Gbits =2GB
GA	24 Gbits =3GB
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G7	128(=2^7) Gbits =16GB
GD	192 Gbits =24GB
G8	256(=2^8) Gbits =32GB
GE	384 Gbits =48GB
G9	512(=2^9) Gbits =64GB
GF	768 Gbits =96GB
T0	1(=2^0) Tbits =128GB
T1	2(=2^1) Tbits =256GB

P/N Decoder for NAND w/ controller ~Details-2

T H G B M 2 G 9 D B F B A I 2 x x x

Symbol	Cell Level
S	2 Level (1 bits/cell)
D	4 Level (2 bits/cell)
T	8 Level (3bits/cell)

Symbol	Stacked die
1~9	1~9die
A	12die
B	16die

Symbol	Design Rule
0	Normal version (0ºC~70ºC)
I	Industrial version (- 25ºC or - 40ºC~85ºC)

Symbol	Design Rule
A	130 nm
B	90 nm
C	70 nm
D	56 nm
E	43 nm
F	32nm
G	24nm A-type
H	24nm B-type

PKG	Symbol	Lead Free	Halogen Free
TSOP	FT	No	No
	TG*	Yes	No
	TA	Yes	Yes
BGA	XB	No	No
	XG*	Yes	No
	BA	Yes	Yes
LGA	-	No	No
	XL*	Yes	No
	LA	Yes	Yes

*Some of the product are Halogen Free with this code.
If necessary, Please ask to Toshiba.

P/N Decoder for NAND w/ controller ~Details-3

T H G B M 2 G 9 D B F B A I 2 x x x

Symbol	TSOP [mm]	LGA [mm]	BGA [mm]
0	12 x 20 x 1.2	12 x 18 x 1.4	12 x 18 x 1.4
1	Reserved	Reserved	12 x 18 x 1.2
2	Reserved	14 x 18 x 1.4	14 x 18 x 1.4
3	Reserved	Reserved	14 x 18 x 1.2
6	Reserved	Reserved	14 x 18 x 1.5
8	Reserved	14 x 18 x 0.9	11.5 x 13 x 1.2
9	Reserved	14 x 18 x 1.0	12 x 16 x 1.2
B	Reserved	Reserved	12 x 16 x 1.4
E	Reserved	Reserved	12 x 16 x 1.2 *1
F	Reserved	Reserved	17 x 22 x 1.4 *1
G	Reserved	Reserved	11.5 x 13 x 1.2 *1
H	Reserved	Reserved	12 x 16 x 1.4 *1
I	Reserved	Reserved	14 x 18 x 1.2 *1
J	Reserved	Reserved	14 x 18 x 1.4 *1
K	Reserved	Reserved	14 x 18 x 1.4 *2

*1: OSP=Organic Solderability Preservatives. *2: Package internal structure optimization.

Change History for Part Number Decoder

Revision	Released Date	Note
1.0	Nov.17'2008	Rev.1.0 is released.
1.1	Nov.27th'2008	To add P/N of NAND with controller
1.2	Dec.10th'2008	Page 5…# of CE for LGA 1 → 1 / 2 Page 9…Lower Temp. coverage : -40°C → -25°C or -40°C
1.3	Sep.24th'2010	To add new P/N rule

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